a substrate, the microstructure being centrally positioned and integrated on the substrate; and

a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

2. (Three Times Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being peripherally positioned and integrated on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

3. (Three Times Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure;

a peripheral circuit comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and

a substrate, the first and second microstructures being integrated on the substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

8. (Three Times Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit comprising a line driver circuit for the passive matrix array;

an associated circuit having a same or a different function as the memory cells;

a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate, wherein the line driver circuit is positioned and electrically connected with the passive matrix array.

9. (Three Times Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit comprising a line driver for the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated, positioned and integrated on the single microstructure, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

10. (Three Times Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a central part of the second microstructure to be integrated; and

a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the second microstructure, wherein the line driver circuit is electrically connected with the passive matrix array.

12. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a microstructure;

separately forming the peripheral circuit on a substrate; and

centrally positioning and integrating the microstructure on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

13. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array centrally disposed on a substrate;

separately forming the peripheral circuit on a microstructure; and

integrating the microstructure on the substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

14. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric

capacitors, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

18. (Three Times Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a central part of the second microstructure to be integrated, wherein the line driver circuit is electrically connected with the passive matrix array.

19. (Three Times Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of microstructures; and